COST Action IC1405
Reversible Computation
Extending Horizons of Computing

Working Group 3 - Reversible Circuit Design
Grant Period 3 report

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COST Action IC1405: Reversible Computation - Extending Horizons of Computing

End-of-the- year report for WG3

This report presents selected results obtained in Working Group 3 of the COST Action IC 1405 on reversible computations in the last grant period. The respective contributions are structured along categories which have been introduced in the WG3 State-of-the-art Report which is accessible through https://github.com/COST-IC1405/wg3-soar-report/blob/master/README.md.

Function Representations and Classes

R. Wille, P. Niemann, A. Zulehner, and R. Drechsler: Decision Diagrams for the Design of Reversible and Quantum Circuits. In International Symposium on Devices, Circuits and Systems (ISDCS), 2018.

Reversible circuits found great interest in the past as an alternative computation paradigm which can be beneficial e.g. for encoder circuits, low power design, adiabatic circuits, verification, and much more. Besides that, reversible circuits provide the basis for many components of quantum circuits, which by themselves emerged as a very promising computing technology that, particularly these days, gains more and more relevance. All that led to a steadily increasing demand for methods that efficiently and correctly design such circuits. Decision diagrams play an important role in the design of conventional circuitry. In the meantime, also their benefits for the design of the newly emerging reversible and quantum circuits become evident. In this overview paper, we review and illustrate past work on decision diagrams for such circuits and sketch corresponding design methods relying on them. By this, we demonstrate how broadly decision diagrams can be employed in this area and what benefits they yield for these emerging technologies.

P. Niemann and R. Wille: Compact Representations for the Design of Quantum Logic. Springer, 2017.

This book discusses modern approaches and challenges of computer-aided design (CAD) of quantum circuits with a view to providing compact representations of quantum functionality. Focusing on the issue of quantum functionality, it presents Quantum Multiple-Valued Decision Diagrams (QMDDs – a means of compactly and efficiently representing and manipulating quantum logic. For future quantum computers, going well beyond the size of present-day prototypes, the manual design of quantum circuits that realize a given (quantum) functionality on these devices is no longer an option. In order to keep up with the technological advances, methods need to be provided which, similar to the design and synthesis of conventional circuits, automatically generate a circuit description of the desired functionality. To this end, an efficient representation of the desired quantum functionality is of the essence. While straightforward representations are restricted due to their (exponentially) large matrix descriptions and other decision diagram-like structures for quantum logic suffer from not comprehensively supporting typical characteristics, QMDDs employ a decomposition scheme that more naturally models quantum systems. As a result, QMDDs explicitly support quantum-mechanical effects like phase shifts and are able to take more advantage of corresponding redundancies, thereby allowing a very compact representation of relevant quantum functionality composed of dozens of qubits. This provides the basis for the development of sophisticated design methods as shown for quantum circuit synthesis and verification.

P. Kerntopf, R. S. Stanković, K. Podlaski,and C. Moraga: Ternary/MV reversible functions with component functions from different equivalence classes. in: International Symposium on Multiple-Valued Logic (ISMVL), 2018.

In an earlier paper the authors considered whether all component functions of a ternary reversible function either can belong to the same equivalent class in some classifications or can have the same property in the sense of classical logic synthesis. In this paper it is shown that there exist ternary/MV reversible functions of any number of variables with all component functions belonging to different P-equivalence classes.

Embedding

A. Zulehner and R. Wille: Pushing the Number of Qubits Below the Minimum: Realizing Compact Boolean Components for Quantum Logic. in: Design, Automation and Test in Europe (DATE), 2018.

Research on quantum computers has gained attention since they are able to solve certain tasks significantly faster than classical machines (in some cases, exponential speed-ups are possible). Since quantum computations typically contain large Boolean components, design automation techniques are required to realize the respective Boolean functions in quantum logic. They usually introduce a significant amount of additional qubits – a highly limited resource. In this work, we propose an alternative method for the realization of Boolean components for quantum logic. In contrast to the current state-of-the-art, we dedicatedly address the main reasons causing the additionally required qubits (namely the number of the most frequently occurring output pattern as well as the number of primary outputs of the function to be realized) and propose to manipulate the function so that both issues are addressed. The resulting methods allow to push the number of required qubits below what is currently considered the minimum.

Synthesis algorithms for reversible functions

A. Zulehner, P. M. N. Rani, K. Datta, I. Sengupta, and R. Wille: Generalizing the Concept of Scalable Reversible Circuit Synthesis for Multiple-valued Logic. in: International Symposium on Multiple-Valued Logic (ISMVL), 2018.

Research on reversible circuits has gained significance due to its application in quantum computations and many further areas such as the design of encoders. At the same time, the use of multiple-valued logic gained importance since this reduces the number of required entities in physical systems (e.g. in a future quantum computer). While most research is still conducted in the Boolean domain, there

exist only few approaches which realize reversible circuits for multiple-valued logic. Moreover, most of the previously proposed solutions for synthesis of multiple-valued reversible circuits are not scalable and consider ternary (i.e. 3-valued circuits) only. Instead of overcoming these issues by developing new synthesis approaches for multiple-valued reversible circuits from scratch, we propose to utilize the recent accomplishments in the design of Boolean reversible circuits and to generalize them for multiple-valued logic. To this end, we discuss how to generalize Quantum Multiple-valued Decision Diagram based (QMDD-based) synthesis – a synthesis approach for Boolean reversible circuits which has been proven to be scalable and which has been used in several recently developed design flows. The discussions eventually show how to bridge the development gap between Boolean and multiple-valued logic for reversible circuits.

F. Hadjam and C. Moraga: Distributed Evolutionary Design of Reversible Circuits. in: Further Improvements in the Boolean Domain ,B. Steinbach (Ed.) , Cambridge Scholars Publishing, 2018, 372-383, ISBN 978-1-5275-0371-7.

A distributed hierarchical evolutionary system, named DRIMEP2, for the design of reversible circuits was earlier successfully introduced. In the present work we extend the concept of distributed evolutionary design algorithm, enlarging DRIMEP2 to a family of distributed systems including the hierarchical model, the Islands Model, and two hybrid architectures: one comprising a hierarchical model with islands at the lower level, and another one consisting of islands of hierarchical models. A set of 17 selected 4-bit reversible benchmarks has been evolved under similar parameter environments for the four studied systems. For each benchmark, 100 independent runs were realized and statistics such as average quantum cost, average successful runs and total execution time were considered in the comparison. The results show that in most cases the straight hierarchical model and the hierarchical model with islands of workers are the best in terms of quantum cost, although all four distributed DRIMEP2 systems obtained a close performance.

Z. Hu, I. Yuriychuk and V. Deibuk: Ternary reversible/quantum latches. in: IEEE First Ukraine Conference on Electrical and Computer Engineering (UKRCON), 2017, 904-907.

Ternary reversible latches on the basis of one- and two-qutrit permutative Muthukrishnan-Stroud (MS) gates were synthesized for the first time. Such gates can be physically implemented on the basis of liquid ion-trap quantum technology. The use of adaptive genetic algorithm allowed designing the circuits of latches that are optimal with respect to quantum cost, number of gates, and delay time. Comparisons of synthesized circuits with known results of other authors were carried out.

J. Jegier: PPRM-based synthesis of reversible logic circuits (in Polish). PhD thesis, Department of Electronics and Information Methods, Warsaw University of Technology, Warsaw, Poland, December 2017, 108 pp.

A PPRM-based synthesis approach is presented in this work which has enabled for reducing quantum cost of circuits - in comparison with the best solutions - by 20% on average -, at the expense of using additional lines in the circuit. Additionally, at the postsynthesis stage, algorithms for solving the known maximum weighted matching problem have been applied – for the first time in the literature – to reduction of quantum cost. Moreover, new sequences of benchmark functions and the circuits implementing them were constructed - again for the first time in the literature –as well as proofs of gate count minimality of these circuits for arbitrary number of variables are presented in the thesis.

M. Lukac, P. Kerntopf, and M. Kameyama: An analytic sifting approach to optimization of LNN reversible circuits. in: International Conference on Information Digital Technologies (IDT,) **13**, 2017, 6 pp.

In this paper an analytic approach to the variable sifting based on weighting of qubits and gates is presented. The proposed scheme allows to optimally sift multi-control single-target reversible gates within a linear number of steps of computation and provides in general smaller amount of SWAP gates required to transform a reversible circuit into a Linear Nearest Neighbor (LNN) model than other competing approaches. The method is analyzed for two different models of implementations,

is verified on experimental data and the results are compared to the state-of-the-art algorithms for the design of LNN circuits.

A. Skorupski: Graphical Method of Reversible Circuits Synthesis. Journal of Electronics and Telecommunications, **63**, no. 3, 2017, 235-240, DOI: 10.1515/eletel-2017-0031.

The paper presents a new approach to designing reversible circuits. The main problem of reversible logic is designing optimal reversible circuits, i.e. circuits with the minimal number of gates implementing the given reversible function. There are many types of reversible gates. Most popular library is the set of three types of gates so called NCT (NOT, CNOT and Toffoli). The method presented in this paper is based only on the NCT gates. A graphical representation of the reversible function called s-map is introduced in the paper. This representation allows to find optimal reversible circuits.

S. Stojković, M. M. Stanković, C. Moraga and R. S. Stanković: FDD-based reversible synthesis by levels. in: Further Improvements in the Boolean Domain ,B. Steinbach (Ed.) , Cambridge Scholars Publishing, 2018, 372-383, ISBN 978-1-5275-0371-7.

Decision diagrams are a data structure suitable for reversible circuit synthesis, since the design procedure is reduced to traversing the diagram and replacement of nodes with reversible modules. Decision diagrams differ with respect to decomposition rules assigned to the nodes. This difference reflects into complexity of reversible modules replacing the nodes in the diagram. In this paper, a comparison of reversible circuits produced from Binary decision diagrams (BDDs), Bidirectional binary decision diagrams (BBDDs), and Functional decision diagrams (FDDs) with different polarity of Davio nodes is presented. Experimental results over benchmark functions show that these diagrams in many cases produce reversible circuits with both smaller quantum cost and number of lines compared to BDDs and BBDDs.

K. Gracki: Reversible Gate and Circuits Descriptions. in: 40th IEEE-SPIE Joint Symposium on Photonics, Web Engineering, Electronics for Astronomy and High Energy Physics Experiments, 2017, 8 pp.

During synthesis of reversible circuits it is needed to use a compact notation of gates in a reversible circuit. The paper presents a method of reversible circuit description. The most popular library is the set of three types of gates called NCT (NOT, CNOT and Toffoli). The presented gate indexing method has been developed for the CNT library of gates.

M. Rawski and P. Szotkowski: Reversible Synthesis of Incompletely Specified Boolean Functions Using Functional Decomposition. in: 40th IEEE-SPIE Joint Symposium on Photonics, Web Engineering, Electronics for Astronomy and High Energy Physics Experiments, 2017, 8 pp.

The paper presents the application of functional decomposition as a crucial step in synthesis of reversible logic that cost-efficiently implements incompletely specified Boolean functions. A decomposition of an incompletely specified Boolean function into a network of smaller sub-functions, subsequently synthesized into reversible blocks and composed into a reversible system, yields significantly better results than direct reversible synthesis of the original, incompletely specified Boolean function. The experimental results presented in the paper demonstrate the potential of the proposed approach.

A. Skorupski: A Method of Reversible Circuits Synthesis Based on S-maps. in: 40th IEEE-SPIE Joint Symposium on Photonics, Web Engineering, Electronics for Astronomy and High Energy Physics Experiments, 2017, 11 pp.

The paper presents an original method to designing reversible circuits. The main problem of reversible circuits synthesis is designing optimal reversible circuits, i.e. circuits with the minimal number of gates implementing the given reversible function. To design reversible circuits a set of gates must be chosen. The most popular library is the set called NCT (NOT, CNOT and Toffoli) which contains three types of gates. The method presented in this paper is based on the CNT gates. A graphical representation of the reversible function called s-map is introduced in the paper. This representation allows to find optimal solutions.

Synthesis algorithms for non-reversible functions

A. Zulehner and R. Wille: One-pass Design of Reversible Circuits: Combining Embedding and Synthesis for Reversible Logic. IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems (TCAD), 2017.

Reversible computation is a heavily investigated emerging technology due to its promising characteristics in low-power design, its application in quantum computations, and several further application areas. The currently established functional synthesis flow for reversible circuits is composed of two distinct steps. First, an embedding process is conducted which makes non-unique output patterns distinguishable by adding further variables. Then, this function is passed to a synthesis method which eventually yields a reversible circuit. However, the separate consideration of the embedding and synthesis tasks leads to significant drawbacks: In fact, embedding is not necessarily conducted in a fashion which is suited for the following synthesis process. In addition, embedding adds further variables to the function to be synthesized which exponentially increases its corresponding representation in the worst case. In this work, we propose one-pass design of reversible circuits, which combines embedding and synthesis. This allows for conducting synthesis with a high degree of freedom, since the embedding that suits best is inherently chosen during synthesis. We propose two solutions (an exact an a heuristic one) following this scheme that improve the currently established synthesis flow by magnitudes in terms of runtime – allowing to synthesize a reversible circuit with a minimum number of lines for some of the frequently considered benchmark functions for the first time. Furthermore, a significant reduction of the costs of the resulting circuits (up to several orders of magnitude) is achieved with this new design flow.

A. Zulehner and R. Wille: Exploiting Coding Techniques for Logic Synthesis of Reversible Circuits. in: Asia and South Pacific Design Automation Conference (ASP-DAC), 2018.

Reversible circuits are composed of a set of circuit lines that are passed through a cascade of reversible gates. Since the number of circuit lines is crucial, functional logic synthesis approaches have been proposed which realize circuits where the number of circuit lines is minimal. However, since the function to be realized is often non-reversible, additional variables have to be added to the function in order to establish reversibility – leading to a significant overhead that affects the scalability of the synthesis method and yields rather complex circuits. In this work, we propose to overcome these problems by exploiting coding techniques in the logic synthesis of reversible circuits. To this end, we propose an intermediate encoding of the output patterns that requires fewer additional inputs and outputs. Using this synthesis scheme allows to perform the majority of the

synthesis on significantly fewer variables and to exploit several don't care values in the code. Experimental evaluations – where we obtain better scalability and circuits with magnitudes fewer costs – confirmed the benefits of the proposed synthesis approach.

Synthesis algorithms based on HDLs

Z. Al-Wardi, R. Wille, and R. Drechsler: Synthesis of Reversible Circuits Using Conventional Hardware Description Languages. in: International Symposium on Multiple-Valued Logic (ISMVL), 2018.

Hardware Description Languages (HDL) facilitate the design of complex circuits and allow for scalable synthesis. While rather established for conventional circuits, HDL-based design of reversible circuits is in its infancy. This motivates the question whether conventional HDLs can also be efficiently used for the design of reversible circuits. This work investigates this question and provides a basis towards a design flow that requires only little knowledge of reversible computation. This eases the acceptance of this non-conventional paradigm amongst designers and stakeholders.

Applications

A. Zulehner, A. Paler, and R. Wille: Efficient Mapping of Quantum Circuits to the IBM QX Architecture. in: Design, Automation and Test in Europe (DATE), 2018.

In March 2017, IBM launched the project IBM Q with the goal to provide access to quantum computers for a broad audience. This allowed users to conduct quantum experiments on a 5-qubit and, since June 2017, also on a 16-qubit quantum computer (called IBM QX2 and IBM QX3, respectively). In order to use these, the desired quantum functionality (e.g. provided in terms of a quantum circuit) has to properly be mapped so that the underlying physical constraints are satisfied – a complex task. This demands for solutions to automatically and efficiently conduct this mapping process. In this paper, we propose such an approach which satisfies all constraints given by the architecture and, at the same time, aims to keep the overhead in terms of additionally required quantum gates minimal. The proposed approach is generic and can easily be configured for future architectures. Experimental evaluations show that the proposed approach clearly outperforms IBM's own mapping solution with respect to runtime as well as resulting costs.

A. Zulehner and R. Wille: Advanced Simulation of Quantum Computations. IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems (TCAD), 2018.

Quantum computation is a promising emerging technology which, compared to conventional computation, allows for substantial speed-ups e.g. for integer factorization or database search. However, since physical realizations of quantum computers are in their infancy, a significant amount of research in this domain still relies on simulations of quantum computations on conventional machines. This causes a significant complexity which current state-of-the-art simulators try to tackle with a rather straight forward array-based representation and by applying massive hardware power. There also exist solutions based on decision diagrams (i.e. graph-based approaches) that try to tackle the exponential complexity by exploiting redundancies in quantum states and operations. However, these existing approaches do not fully exploit redundancies that are actually present. In this work, we revisit the basics of quantum computation, investigate how corresponding quantum states and quantum operations can be represented even more compactly, and, eventually, simulated in a more efficient fashion. This leads to a new graph-based simulation approach which outperforms state-of-

the-art simulators (array-based as well as graph-based). Experimental evaluations show that the proposed solution is capable of simulating quantum computations for more qubits than before, and in significantly less run-time (several magnitudes faster compared to previously proposed imulators). An implementation of the proposed simulator is publicly available online at http://www.jku.at/iic/eda/quantum_simulation.

Giulia Meuli, Mathias Soeken, Martin Roetteler, Nathan Wiebe, Giovanni De Micheli: A best-fit mapping algorithm to facilitate ESOP-decomposition in Clifford+T quantum network synthesis. ASP-DAC, 2018, 664-669

Currently, there is a large research interest and a significant economical effort to build the first practical quantum computer. Such quantum computers promise to exceed the capabilities of conventional computers in fields such as computational chemistry, machine learning and cryptanalysis. Automated methods to map logic designs to quantum networks are crucial to fully realizing this dream, however, existing methods can be expensive both in computational time as well as in the size of the resultant quantum networks. This work introduces an efficient method to map reversible single-target gates into a universal set of quantum gates (Clifford+T). This mapping method is called best-fit mapping and aims at reducing the cost of the resulting quantum network. It exploits fc-LUT mapping and the existence of clean ancilla qubits to decompose a large single-target gate into a set of smaller single-target gates. In addition, this work proposes a post-synthesis optimization method to reduce the cost of the final quantum network, based on two cost-minimization properties. Results show a cost reduction for the synthesized EPFL benchmark up to 53% in the number T gates.

Mathias Soeken, Thomas Haener, Martin Roetteler: Programming quantum computers using design automation. DATE, 2018, 137-146

Recent developments in quantum hardware indicate that systems featuring more than 50 physical qubits are within reach. At this scale, classical simulation will no longer be feasible and there is a possibility that such quantum devices may outperform even classical supercomputers at certain tasks. With the rapid growth of qubit numbers and coherence times comes the increasingly difficult challenge of quantum program compilation. This entails the translation of a high-level description of a quantum algorithm to hardware-specific low-level operations which can be carried out by the quantum device. Some parts of the calculation may still be performed manually due to the lack of efficient methods. This, in turn, may lead to a design gap, which will prevent the programming of a quantum computer. In this paper, we discuss the challenges in fully-automatic quantum compilation. We motivate directions for future research to tackle these challenges. Yet, with the algorithms and approaches that exist today, we demonstrate how to automatically perform the quantum programming flow from algorithm to a physical quantum computer for a simple algorithmic benchmark, namely the hidden shift problem. We present and use two tool flows which invoke RevKit. One which is based on ProjectQ and which targets the IBM Quantum Experience or a local simulator, and one which is based on Microsoft's quantum programming language Q#.

W. Castryck, J. Demeyer, A. De Vos, O. Keszocze, M. Soeken: Translating between the roots of identity in quantum circuits. in: International Symposium on Multiple-Valued Logic (ISMVL), 2018.

The Clifford+T quantum computing gate library for single qubit gates can create all unitary matrices that are generated by the group <H, T>. The matrix T can be considered the fourth root of Pauli Z, since $T^4 = Z$ or also the eighth root of the identity I. The Hadamard matrix H can be used to translate between the Pauli matrices, since $(HTH)^4$ gives Pauli X. We are generalizing both these roots of the Pauli matrices (or roots of the identity) and translation matrices to investigate the groups they generate: the so-called Pauli root groups. In this work we introduce a formalization of such groups, study finiteness and infiniteness properties, and precisely determine equality and subgroup relations.

A. Paler, A. G. Fowler, and R. Wille: Synthesis of Arbitrary Quantum Circuits to Topological Assembly: Systematic, Online and Compact. Scientific Reports, 7(1), 2017.

It is challenging to transform an arbitrary quantum circuit into a form protected by surface code quantum error correcting codes (a variant of topological quantum error correction), especially if the goal is to minimise overhead. One of the issues is the efficient placement of magic state distillation sub circuits, so-called distillation boxes, in the space-time volume that abstracts the computation's required resources. This work presents a general, systematic, online method for the synthesis of such circuits. Distillation box placement is controlled by so-called schedulers. The work introduces a greedy scheduler generating compact box placements. The implemented software, whose source code is available online, is used to illustrate and discuss synthesis examples. Synthesis and optimisation improvements are proposed.

A. Paler, A. G. Fowler, and R. Wille: Online scheduled execution of quantum circuits protected by surface codes. Quantum Information & Computation (QIC), 2017.

Quantum circuits are the preferred formalism for expressing quantum information processing tasks. Quantum circuit design automation methods mostly use a waterfall approach and consider that high level circuit descriptions are hardware agnostic. This assumption has lead to a static circuit perspective: the number of quantum bits and quantum gates is determined before circuit execution and everything is considered reliable with zero probability of failure. Many different schemes for achieving reliable fault-tolerant quantum computation exist, with different schemes suitable for different architectures. A number of large experimental groups are developing architectures well suited to being protected by surface quantum error correcting codes. Such circuits could include unreliable logical elements, such as state distillation, whose failure can be determined only after their actual execution. Therefore, practical logical circuits, as envisaged by many groups, are likely to have a dynamic structure. This requires an online scheduling of their execution: one knows for sure what needs to be executed only after previous elements have finished executing. This work shows that scheduling shares similarities with place and route methods. The work also introduces the first online schedulers of quantum circuits protected by surface codes. The work also highlights scheduling efficiency by comparing the new methods with state of the art static scheduling of surface code protected fault-tolerant circuits.

X. Cui, S. M. Saeed, A. Zulehner, R. Wille, K. Wu, R. Drechsler, and R. Karri: On the Difficulty of Inserting Trojans in Reversible Computing Architectures. IEEE Transactions on Emerging Topics in Computing (TETC), 2018.

Fabrication-less design houses outsource their designs to third-party foundries to lower fabrication cost. However, this creates opportunities for a rogue in the semiconductor foundry to introduce hardware Trojans, which stay inactive most of the time and cause unintended consequences to the system when triggered. Hardware Trojans in traditional CMOS-based circuits have been studied, and Design-for-Trust (DFT) techniques have been proposed to detect them. Different from traditional circuits in many ways, reversible circuits implement one-to-one input/output mappings. We will investigate the security implications of reversible circuits with a particular focus on susceptibility to hardware Trojans. This work studies reversible functions implemented using reversible circuits as well as irreversible functions embedded in reversible circuits.

S. M. Saeed, N. Mahendran, A. Zulehner, R. Wille, and R. Karri: Identifying Synthesis Approaches for IP Piracy of Reversible Circuits. in: International Conference on Computer Design (ICCD), 2017.

Reversible circuits are vulnerable to intellectual property and integrated circuit piracy. To show these vulnerabilities, a detailed understanding on how to identify the function embedded in a reversible circuit is crucial. To obtain the embedded function, one needs to know the synthesis approach used to generate the reversible circuit in the first place. We present a machine learning based scheme to identify the synthesis approach using telltale signs in the design.

List of All Publications

- R. Wille, P. Niemann, A. Zulehner, and R. Drechsler: Decision Diagrams for the Design of Reversible and Quantum Circuits. In International Symposium on Devices, Circuits and Systems (ISDCS), 2018.
- P. Niemann and R. Wille: Compact Representations for the Design of Quantum Logic. Springer, 2017.
- P. Kerntopf, R. S. Stanković, K. Podlaski,and C. Moraga: Ternary/MV reversible functions with component functions from different equivalence classes. in: International Symposium on Multiple-Valued Logic (ISMVL), 2018.
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