ICT COST Action IC1405

COST Action IC1405
Reversible Computation
Extending Horizons of Computing

Working Group 3 - Reversible Circuit Design

Grant Period 2 report

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This report presents selected results obtained in Working Group 3 of the COST Action IC 1405 on reversible computations in the last grant period. The respective contributions are structured along categories which have been introduced in the WG3 State-of-the-art Report which is accessible through https://github.com/COST-IC1405/wg3-soar-report/blob/master/README.md.

Function Representations and Classes

P. Niemann, A. Zulehner, R. Wille, and R. Drechsler: Efficient construction of QMDDs for irreversible, reversible, and quantum functions, in: *RC* **9**, 2017.

In reversible as well as quantum computation, unitary matrices (so-called transformation matrices) are employed to comprehensively describe the respectively considered functionality. Due to the exponential growth of these matrices, dedicated and efficient means for their representation and manipulation are essential in order to deal with this complexity and handle reversible/quantum systems of considerable size. To this end, Quantum Multiple-Valued Decision Diagrams (QMDDs) have shown to provide a compact representation of those matrices and have proven their effectiveness in many areas of reversible and quantum logic design such as embedding, synthesis, or equivalence checking. However, the desired functionality is usually not provided in terms of QMDDs, but relies on alternative representations such as Boolean Algebra, circuit netlists, or quantum algorithms. In order to apply QMDD-based design approaches, the corresponding QMDD has to be constructed first - a gap in many of these approaches. In this paper, we show how QMDD representations can efficiently be obtained for Boolean functions, both reversible and irreversible ones, as well as general quantum functionality.

P. Kerntopf, C. Moraga,K. Podlaski, and R.S. Stanković: Towards classification of reversible functions with homogeneous component functions. in: *IWBP* **12**, 2016, 21-28.

Although during the last 15 years the field of reversible circuit synthesis has been intensively studied very few publications have been devoted to classification of reversible functions. In the paper we consider whether all component functions of a reversible function either can belong to the same equivalent class in some classifications or can have the same property in the sense of classical logic synthesis. This problem has a direct relationship to studying different aspects of classification of reversible functions. We have calculated all NPN-equivalence classes of balanced Boolean functions up to 4 variables (never published) and all NPNP-equivalence classes of reversible functions of 3 variables (correcting earlier data). We also present component functions of any number of variables belonging to the same equivalence class or having the same property.

P. Kerntopf, K. Podlask,and C. Moraga,and R.S. Stanković: Study of reversible ternary functions with homogeneous component functions. in: *ISMVL* **47**, 2017, 191-196.

In an earlier paper the authors considered whether all component functions of a reversible Boolean function either can have the same property in the sense of classical logic synthesis or can belong to the same equivalent class under some equivalent relations. This problem has a direct relationship to studying different aspects of classification of reversible functions. In this paper solutions of the

problem are presented for reversible ternary functions. It is shown that for linear/affine functions the results in binary and ternary cases differ significantly.

P. Kerntopf.,C. Moraga,K. Podlaski, and R.S. Stanković: Towards classification of reversible functions. in: *Further Improvements in the Boolean Domain*, Bernd Steinbach (ed.), Cambridge Scholars Publishing, 2017, 21 pp., in print.

In this chapter reversible functions with component functions which have the same known property or belong to the same equivalence class in some classifications are studied. Investigating such problems may lead to new classifications which would be interesting from the point of view of reversible circuit synthesis. The presented results show that for $n \geq 3$ there exist reversible Boolean functions having all component functions being homogeneous and non-degenerate.

K. Podlaski: Cycle structures of the reversible Hidden Weighted Bit function. in: *RM Workshop* **13**, 2017, 73-78.

Reversible Hidden Weighted Bit function (HWBnxn) is very often used as one of the "hardest" benchmarks for synthesis algorithms. In the area of reversible synthesis some of the best known algorithms are based on cycle representation of reversible functions. The structure of cycles for a given function has an impact on size of the circuit implemented with usage of cycle-based methods. Although many papers have been published on reversible functions there are no works focused on cycle structure of HWBnxn. This paper presents some results on analysis of cycles for HWBnxn functions. These results can be used to develop new synthesis algorithms or function complexity measures.

Gate Libraries

C. Moraga: Design of p-valued Deutsch quantum gates with multiple control signals and mixed polarity, in: *Reversible Computation,* S. Devitt, I. Lanese, Eds., LNCS 9720, 175-180, Springer International Publishing AG, Switzerland, 2016.

This paper presents a detailed study of the realization of p–valued Deutsch quantum gates with $n > 2$ controlling signals, both under conjunctive and disjunctive control, and including zero or mixed polarity of the controlling signals. It is shown that the realization complexity is in $O(pn - 1)$. The realization comprises only Muthukrishnan-Stroud elementary quantum gates.

C. Moraga: Quantum p-valued Toffoli and Deutsch gates with conjunctive or disjunctive mixed polarity control, in: *ISMVL* **46**, 2016, 241-246.

In this paper the models of reversible Toffoli and quantum Deutsch gates are extended to the p-valued domain. Their structural parameters are determined and their behavior is proven. Both conjunctive and disjunctive control strategies with positive and mixed polarities are introduced for the first time in a p-valued domain. The design is based on elementary Muthukrishnan-Stroud quantum gates, hence the realizability of the extended gates in the context of ion traps should be possible.

M. Lukac, C. Moraga,and M. Kameyama: The CnF logic gates derived from CnNOT gates. in: *IWBP* **12**, 2016, 29-34.

The C2NOT gate is one of the simplest Turing universal reversible logic gate. Implemented in quantum circuit technologies in the CV/CV†/CNOT model the C2NOT gate is in general built by two components: a classical set of single variables controlled CV/CV† gates implementing some quantum function interference pattern and a set of quantum gates implementing a quantum function controlled by a symmetric like function. These two components allow to overcome the limitation of the inability of classical reversible two qubit gates in generating a Turing universal function. In this paper we analyze both of these components and study what other functions can be created using this two qubit gates. The application of this study is the possible use of low cost reconfiguration of a reversible or quantum FPGA.

M. Yüksel; S.O. Erbil, A.B. Ari, and M.S. Hanay: Design and fabrication of CSWAP gate based on nano-electromechanical systems, in: *RC* **8**, 2016.

In order to reduce undesired heat dissipation, reversible logic offers a promising solution where the erasure of information can be avoided to overcome the Landauer limit. Among the reversible logic gates, Fredkin (CSWAP) gate can be used to compute any Boolean function in a reversible manner. To realize reversible computation gates, Nano-electromechanical Systems (NEMS) offer a viable platform, since NEMS can be produced en masse using microfabrication technology and controlled electronically at high-speeds. In this work-in-progress paper, design and fabrication of a NEMS-based implementation of a CSWAP gate is presented. In the design, the binary information is stored by the buckling direction of nanomechanical beams and CSWAP operation is accomplished through a mechanism which can selectively allow/block the forces from input stages to the output stages. The gate design is realized by fabricating NEMS devices on a Silicon-on-Insulator substrate.

M. Soeken, N. Abdessaied,and G. De Micheli: Enumeration of reversible functions and its application to circuit complexity, in: *RC* **8**, 2016, 255-270.

A new theoretical result relates Boolean function classification for reversible functions to the multiple-controlled Toffoli gate library.

Embedding

A. Zulehner and R. Wille: Make It reversible: Efficient embedding of non-reversible functions. in: *DATE*, 2017.

Reversible computation became established as a promising concept due to its application in various areas like quantum computation, energy-aware circuits, and further areas. Unfortunately, most functions of interest are non-reversible. Therefore, a process called embedding has to be conducted to transform a non-reversible function into a reversible one – a coNP-hard problem. Existing solutions suffer from the resulting exponential complexity and, hence, are limited to rather small functions only. In this work, an approach is presented which tackles the problem in an entirely new fashion. We divide the embedding process into matrix operations, which can be conducted efficiently on a certain kind of decision diagram. Experiments show that improvements of several orders of magnitudes can be achieved using the proposed method. Moreover, for many benchmarks exact results can be obtained for the first time ever

Synthesis algorithms for reversible functions

A. Zulehner and R. Wille: Improving synthesis of reversible circuits: Exploiting redundancies in paths and nodes of QMDD,.in: *RC* **9**, 2017.

In recent years, reversible circuits have become an established emerging technology through their variety of applications. Since these circuits employ a completely different structure from conventional circuitry, dedicated functional synthesis algorithms have been proposed. Although scalability has been achieved by using approaches based on decision diagrams, the resulting circuits employ a significant complexity measured in terms of quantum cost. In this paper, we aim for a reduction of this complexity. To this end, we review QMDD-based synthesis. Based on that, we propose optimizations that allow for a substantial reduction of the quantum costs by jointly considering paths and nodes in the decision diagram that employ a certain redundancy. In fact, in our experimental evaluation, we observe substantial improvements of up to three orders of magnitudes in terms of runtime and up to six orders of magnitudes (a factor of one million) in terms of quantum cost.

F. Hadjam and C. Moraga: Distributed RIMEP2: a comparative study between a hierarchical model and the islands model in the context of reversible circuits design. in: *IWBP* **12**, 2016, 13-20.

A distributed hierarchical evolutionary system, named DRIMEP2, for the design of reversible circuits was earlier successfully introduced. In the present work we extend the concept of distributed evolutionary design algorithm, enlarging DRIMEP2 to a family of distributed systems including the hierarchical model, the Island Model, and two hybrid architectures: one comprising a hierarchical model with islands at the lower level, and another one consisting of islands of hierarchical models. A set of 17 randomly chosen 4-bit reversible benchmarks has been evolved under similar parameter environments for the four studied systems. For each benchmark, 100 independent runs were realized and statistics such as “average quantum cost”, “average successful runs” and “total execution time” were considered in the comparison. The results show that in most cases the straight hierarchical model and the hierarchical model with islands of workers are the best in terms of “quantum cost”, although all four distributed DRIMEP2 systems obtained a close performance.

S. Stojković,C. Moraga, M.M. Stanković, R.S. Stanković: Procedure for FDD-based reversible synthesis by levels, in: *IWBP* **12**, 2016, 5-12.

Decision diagrams are a data structure suitable for reversible circuit synthesis, since the design procedure is reduced to traversing the diagram and replacement of nodes with reversible modules. Decision diagrams differ with respect to decomposition rules assigned to the nodes. This difference reflects into complexity of reversible modules replacing the nodes in the diagram. In this paper, we compare reversible circuits produced from Binary decision diagrams (BDDs), Bidirectional binary decision diagrams (BBDDs), and Functional decision diagrams (FDDs) with different polarity of Davio nodes. Experimental results over benchmark functions show that these diagrams in many cases produce reversible circuits with both smaller quantum cost and number of lines compared to BDDs and BBDDs.

J. Jegier and P. Kerntopf: Gate count minimal reversible circuits, in: *Problems and New Solutions in the Boolean Domain*, Cambridge Scholars Publishing, Bernd Steinbach (ed.), 2016, 342-355.

A few sequences of reversible functions of an arbitrary number of variables, e.g., hwbn and nth prime inc, have been proposed as benchmarks, but these functions are quite complex and no minimal gate count or minimal quantum cost circuits are known for them for n > 4. Thus, developing methods of constructing functions with known minimal circuits is needed. In this paper, two infinite sequences of functions of any number of variables are presented for which we have constructed gate count minimal circuits (proofs of their minimality are given).

K. Podlaski: Reversible circuit synthesis using binary decision diagrams, in: *MIXDES* **23**, 2016, 235-238.

In this paper a new implementation of the known transformation based algorithm is presented. The existing transformation based algorithms use truth tables during computation. This leads to memory restrictions. On the other hand any Boolean function can be represented using Binary Decision Diagrams (BBD). This representation is more compact and uses less memory than truth table representation. The presented new implementation of the transformation based algorithm can be used for synthesis of much larger reversible functions than the original version of the algorithm.

M. Soeken, G.W. Dueck, and D.M. Miller: A fast symbolic transformation based algorithm for reversible logic synthesis, *RC* **8**, 2016, 307-321.

A symbolic variant of the transformation based synthesis algorithm has been presented. Two algorithms are presented, one is based on binary decision diagrams and another one on Boolean satisfiability. It allows to overcome the exponential time and memory requirements of the original explicit algorithm for some functions. Both algorithms have open source implementations in RevKit (command: tbs).

J. Jegier and P. Kerntopf: PPRM-based approach to synthesis of reversible functions, in: *40th IEEE-SPIE Joint Symposium on Photonics, Web Engineering, Electronics for Astronomy and High Energy Physics Experiments*, 2017.

This work proposes a PPRM-based technique for the synthesis of reversible circuits with reduced quantum cost (QC) in generated circuits. Initially, a PPRM cube-list structure is provided as input. Next, the PPRM cubes shared by coordinate functions of a given reversible function are grouped together and each cube is translated to a group of Toffoli reversible gates, similarly to ESOP-based methods. Experimental results show that for important benchmarks with up to 17 variables the presented approach generates circuits with smaller QC than the most successful previous approaches.

J. Jegier and P. Kerntopf: Application of the maximum weighted matching to quantum cost reduction in reversible circuits. in: *MIXDES*, 2017.

In this paper the maximum weighted matching (PMWM) method, well-known from the graph theory, is applied to reduction of quantum cost (QC) in reversible sub-circuits with a common target line. In this way, possibility of application of the PMWM method to optimization of QC is showed for the first

time in literature on reversible circuit synthesis. Experimental results have shown that this approach leads to substantial reduction of QC.

M. Lukac,P. Kerntopf, and M. Kameyama: An analytic sifting approach to optimization of LNN reversible circuits. in: *RM* **13**, 2017, 87-92.

In this paper an analytic approach to the variable sifting based on weighting of qubits and gates is presented. The proposed scheme allows to optimally sift multi-control single-target reversible gates within a linear number of steps of computation. In general, it provides smaller amount of SWAP gates required to transform a reversible circuit into a Linear Nearest Neighbor (LNN) model than other approaches. The method is analyzed for two different models of implementation and verified on many benchmarks. The experimental results are compared to state-of-the-art algorithms for design of LNN circuits.

Synthesis algorithms for nonreversible functions

I. Lemberski: Asynchronous logic implementation based on factorized DIMS, in: *Journal of Circuits, Systems and Computer* **26**, 2017, 9 pp.

One of popular methods of asynchronous logic implementation is based on so called Delay-Insensitive-Minterm-System (DIMS), where a sum-of-minterms function is given and each minterm is represented using a state-holding (C-) element. However, such implementation is rather expensive since minterm minimization is not allowed. The structure, called factorized DIMS is proposed. It is shown that under realistic delay limitation, instead of sum-of-minterms, strong indication can be ensured for the sum of mutually orthogonal product terms resolved into factorized form. It reduces significantly implementation complexity.

M. Soeken, M. Roetteler, N. Wiebe, and G. De Micheli: Design automation and design space exploration for quantum computers, *DATE* 2017, 470-475.
M. Soeken, M. Roetteler, N. Wiebe, and G. De Micheli: Hierarchical reversible logic synthesis using LUTs,in: *DAC*, 2017.

It has been demonstrated that by combining existing reversible logic synthesis methods with conventional logic synthesis algorithms, it is possible to create scalable design flows for reversible logic with application to quantum computing [SRWM17a]. Input is a Verilog gate level netlist, which is then optimised and resynthesised to meet the requirements of various reversible logic synthesis algorithms. The choice of the underlying reversible logic synthesis algorithm allows design space elaboration by trading off the number of qubits to the number of quantum operations. Based on this work, a new reversible logic synthesis algorithm called LUT-based hierarchical reversible logic synthesis (LHRS) has been presented [SWRM17b]. An open source of the synthesis algorithm is available in RevKit (command: lhrs). The research resulted from a newly commenced collaboration with Microsoft (StationQ, QuArC).

A. Zulehner and R. Wille. Skipping Embedding in the Design of Reversible Circuits. in: *ISMVL* **47**, 2017, 173-178.

Synthesis of reversible circuits finds application in many promising domains but has to deal with the fact that the underlying circuits require a unique mapping from the inputs to the outputs. Existing solutions addressed this problem by additionally performing a so-called embedding process prior to synthesis or by naively mapping building blocks of conventional logic to their corresponding reversible counterparts. This leads to solutions that either suffer from limited scalability or yield circuits with a huge number of additionally required circuit lines. In this work, we conduct investigations to overcome these problems. To this end, we simply ignore the fact that an arbitrary Boolean function to be synthesized might be non-reversible and deal with the resulting problem of ensuring a unique input/output mapping during the actual synthesis process. Experimental evaluations indicate that, following this approach, could provide the basis for an alternative synthesis scheme that allows for synthesizing arbitrary Boolean functions in reasonable time and without the need of a prior embedding process.

Synthesis algorithms based on HDLs

Z. Al-Wardi, R. Wille, and R. Drechsler: Extensions to the reversible hardware description language SyReC. In: *ISMVL* **47**, 2017, 185-190.

Hardware Description Languages (HDL) are proposed to facilitate the design of complex circuits and to allow for scalable synthesis. While rather established for conventional circuits, HDLs for the design and synthesis of reversible circuits are at the beginning. SyReC is a representative of such an HDL which already has successfully be applied to realize complex functionality in reversible logic. Nevertheless, the grammar and, by this, the functional scope of this language is rather limited. In this work, we propose extensions to the SyReC HDL which will enhance the usability of the language. For each extension, we additionally provide corresponding synthesis schemes. Overall, this yields a new (extended) SyReC HDL, which will simplify the design and realization of corresponding circuits.

Z. Al-Wardi, R. Wille, and R. Drechsler: Towards VHDL-based design of reversible circuits, in: *RC* **9**, 2017.

Hardware Description Languages (HDL) facilitate the design of complex circuits and allow for scalable synthesis. While rather established for conventional circuits, HDLs for reversible circuits are in their infancy and usually require a deep understanding of the reversible computing concepts. This motivates the question whether reversible circuits can also efficiently be designed with conventional HDLs, such as VHDL. This work discusses this question. By this, it provides the basis towards a design ow that requires no or only little knowledge of the reversible computation paradigm which could ease the acceptance of this non-conventional computation paradigm amongst designers and stakeholders.

R. Wille, O. Keszocze, L. Othmer, M. K. Thomsen, and R. Drechsler: Generating and checking control logic in the HDL-based design of reversible circuits, in: *ISED*, 2016.

Although different from the conventional computing paradigm, reversible computation received significant interest due to its applications in various (emerging) technologies. Here, computations can be executed not only from the inputs to the outputs, but also in the reverse direction. This leads to

significantly different design challenges to be addressed. In this work, we consider problems that occur when describing a reversible control flow using Hardware Description Languages (HDLs). Here, the commonly used conditional statements must, in addition to the established if-condition for forward computation, be provided with an additional fi-condition for backward computation. Unfortunately, deriving correct and consistent fi-conditions is often not obvious. Moreover, HDL descriptions exist which may not be realized with a reversible control flow at all. In this work, we propose automatic solutions which generate the required fi-conditions and check whether a reversible control flow indeed can be realized. The solution utilizes predicate transformer semantics based on Hoare logic. This has exemplary been implemented for the reversible HDL SyReC and evaluated with a variety of circuit description examples. The proposed solution constitutes the first automatic method for these important designs steps in the domain of reversible circuit design.

Applications

A. Zulehner and R. Wille: Taking one-to-one mappings for granted: Advanced logic design of encoder circuits. in: *DATE*, 2017.

Encoders play an important role in many areas such as memory addressing, data demultiplexing, or for interconnect solutions. However, design solutions for the automatic synthesis of corresponding circuits suffer from various drawbacks, e.g. they are often not scalable, do not exploit the full degree of freedom, or are applicable to realize certain codes only. All these problems are caused by the fact that existing design solutions have to explicitly guarantee a one-to-one mapping. In this work, we propose an alternative design approach which relies on dedicated description means for both, the specification of an encoder as well as its circuit. Based on that, synthesis can be conducted without the need to explicitly take care of guaranteeing one-to-one mappings. Experiments show that this indeed overcomes the drawbacks of current design solutions and leads to an improvement in the resulting number of gates by up to 92%.

A. Zulehner, S. Gasser, and R. Wille: Exact global reordering for nearest neighbor quantum circuits using A*. in: *RC* **9**, 2017.

Since for certain realizations of quantum circuits only adjacent qubits may interact, qubits have to be frequently swapped - leading to a significant overhead. Therefore, optimizations such as exact global reordering have been proposed, where qubits are reordered such that the overall number of swaps is minimal. However, to guarantee minimality all n! possible permutations of qubits have to be considered in the worst case { which becomes intractable for larger circuits. In this work, we tackle the complexity of exact global reordering using an A* search algorithm. The sophisticated heuristics for the search algorithm proposed in this paper allow for solving the problem in a much more scalable fashion. In fact, experimental evaluations show that the proposed approach is capable of determining the best order of the qubits for circuits with up to 25 qubits, whereas the recent state-of-the-art already reaches its limits with circuits composed of 10 qubits.

A. De Vos, and S.De Baerdemacker: Block-ZXZ synthesis of an arbitrary quantum circuit. in: *Physical Review A*, 2016.

At the Universiteit Gent (Belgium), in 2016, De Vos and De Baerdemacker [1] studied the unification of quantum circuit design and classical reversible circuit design. Thanks to the 2015 Führ and Rzeszotnik decomposition of an arbitrary unitary matrix, they succeeded in finding two (dual) synthesis methods for quantum circuits. One of them turns out to have the synthesis of classical circuits as a special case. This leads to a unification of quantum and classical computing.

C. Moraga: Aspects of reversible and quantum computing in a p-valued domain. in: *IEEE JETCAS* **6**, 2016, 44-52.

This work presents basic aspects of non-binary reversible and quantum computing in a p-valued environment, since there are no physical reasons for quantum computing to be necessarily binary. A "quantum technology" is not yet available, but different alternatives at the level of laboratory experiments are promising. A theoretical background is needed to face the challenge of designing circuits for quantum computing. Pauli matrices are introduced in the p-valued domain and their properties are explained. The Vilenkin-Chrestenson matrix is shown to produce superposition of states. Entanglement of quantum states in the p-valued environment is introduced and its measurement effect is illustrated. It is shown that in the p-valued domain, the binary Toffoli gate may be given different generalizations with different functionalities. An ancillary-free realization of a new generalized p-valued Toffoli gate based on Muthukrishnan-Stroud elementary gates is presented, its functionality is extended to two kinds of control, and a proof of its performance is given.

M. Lukac, M. Kameyama, M. Perkowski,P. Kerntopf, C. Moraga: Fault models in reversible and quantum circuits, in: *Advances in Unconventional Computing*, A. Adamatzky, Ed., Springer, 2016.

In this chapter we describe faults that can occur in reversible circuit as compared to faults that can occur in classical irreversible circuits. Because there are many approaches from classical irreversible circuits that are being adapted to reversible circuits, it is necessary to analyze what faults that exists in irreversible circuits can appear in reversible circuit as well. Thus we focus on comparing faults that can appear in classical circuit technology with faults that can appear in reversible and quantum circuit technology. The comparison is done from the point of view of information reversible and information irreversible circuit technologies. We show that the impact of reversible computing and quantum technology strongly modifies the fault types that can appear and thus the fault models that should be considered. Unlike in the classical non-reversible transistor based circuits, in reversible circuits it is necessary to specify what type of implementation technology is used as different technologies can be affected by different faults. Moreover, the level of faults and their analysis must be revised to precisely capture the effects and properties of quantum gates and quantum circuits that share several similarities with reversible circuits. By not doing so the available testing approaches adapted from classical circuits would not be able to properly detect relevant faults. In addition, if the classical faults are directly applied without revision and modifications, the presented testing procedure would be testing for such faults that cannot physically occur in the given implementation of reversible circuits. The observation and analysis of these various faults presented in this chapter clearly demonstrates what faults can occur and what faults cannot occur in various reversible technologies. Consequently the results from this chapter can be used to design more precise tests for reversible logic circuits. Moreover the clearly described differences between faults

occurring in reversible and irreversible circuits means that new algorithms for fault detection should be implemented specifically for particular reversible technologies.

M. Bryk, K. Gracki, P. Kerntopf, M. Pawłowski, and A. Skorupski: Encryption using reconfigurable reversible logic gate and its simulation in FPGAs, in: *MIXDES* **23**, 2016, 203-206.

This paper presents a solution to designing encryption schemes based entirely on reversible logic. In our solution a building block of an encryption scheme is a cascade of 4-input reversible gates which can perform any reversible 4-variable function. For this purpose a reconfigurable reversible gate has been proposed. The design of such a reconfigurable gate built from standard reversible gates, i.e. NOT, CNOT, Toffoli and Fredkin gates, is presented.

List of All Publications

- Z. Al-Wardi, R. Wille, and R. Drechsler: Extensions to the reversible hardware description language SyReC. In: ISMVL 47, 2017, 185-190.
- Z. Al-Wardi, R. Wille, and R. Drechsler: Towards VHDL-based design of reversible circuits, in: RC 9, 2017.
- M. Bryk, K. Gracki, P. Kerntopf, M. Pawłowski, and A. Skorupski: Encryption using reconfigurable reversible logic gate and its simulation in FPGAs, in: MIXDES 23, 2016, 203-206.
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